

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

METHOD FOR FORMING ROBUST SOLDER INTERCONNECT
STRUCTURES BY REDUCING EFFECTS OF SEED LAYER
UNDERETCHING

Application Number :

Confirmation Number:

First Named Applicant: Kamalesh Srivastava

Attorney Docket Number: FIS920030359US1

Art Unit:

Examiner:

Search string: (5462638 or 5486282 or 5796168 or 5620611 or 5937320 or 6293457 or 6468413
.pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5462638	1995-10-31	DATTA, ET AL.			
	2	5486282	1996-01-23	DATTA, ET AL.			
	3	5796168	1998-08-18	DATTA, ET AL.			
	4	5620611	1997-04-15	DATTA, ET AL.			
	5	5937320	1999-08-10	ANDRICACOS, ET AL.			
	6	6293457	2001-09-25	SRIVASTAVA, ET AL.			
	7	6468413	2002-10-22	FANTI, ET AL.			

Signature

Examiner Name	Date